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MULTISHIP TECHNOLOGY - A METHOD OF INCREASING THE PACKING DENSITY WHILE SIMULTANEOUSLY DECREASING THE ASSEMBLY EXPENSE

by

H. J. Hanke

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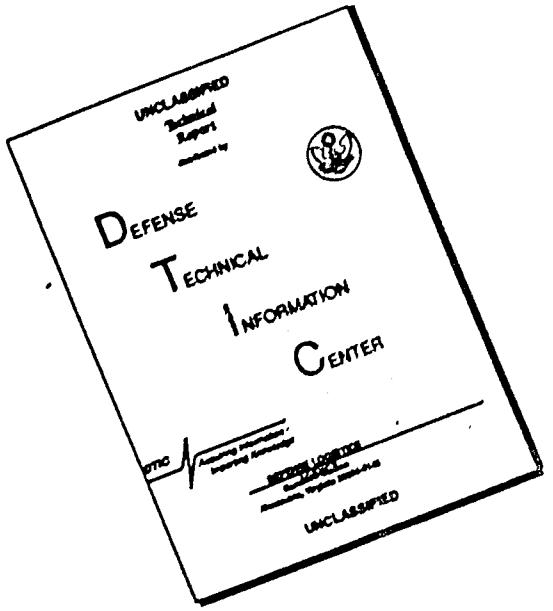

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By: H. J. Hanke

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Multichip technology - a method of increasing the packing density while simultaneously decreasing the assembly expense

H. J. Hanke /209

A specific characteristic of the development of microelectronics of the 70's is, aside from the increasing degree of integration, the development and mass production of integrated elements for all classes of electronic instruments, i.e., for digital as well as analogue instrument ideas.

With the completion of semi-conductor block technology, the possibilities for realization of highly integrated elements were created. Today there are technologies available internationally for bipolar as well as for unipolar technology. With these technologies we achieve , on the one hand, larger gains through simplification of the technological process - as for example for the Trimask process, the silicon gate technique, the ion-implantation MOS technique, or the SATC and Planox procedures. On the other hand we achieve higher packing densities and switching velocities by means of new isolation methods as the CDI-process, the isoplanar processes, as well as the V-ATE-process

and the VIP-process.

The necessity of realizing higher degrees of integration is based primarily on the necessity of reducing the assembly and sealing costs in cycle II of element production, in addition to the demand for increasing the switching velocities by reducing the signal propagation times (shortening the connecting circuit). An analysis of the costs for the producer of integrated elements shows that about 60% of the total production costs for an element rest on the assembly processes of cycle II, i.e., chip assembly and connection contacting as well as capping. In an analagous manner, for the instrument producer the costs for the logical connection of the elements for complex function units dominate, due to the necessary wiring. Thus for the central unit of the computer R 40 about 65% of the costs are material costs for multi-layer-plates and plug connectors; the labor costs are less than 5% of the total costs.

The purely monolithic solution for increasing the degree of integration of the elements, through increasing the degree of integration of the chip while simultaneously changing from chips of the switching circuit method to chips of the function method, has technological limits.

These limits are set by the following: due to the manifold of the necessary cross connections, a many-planar wiring is necessary on the chip; and due to the decreasing yield (due to the larger probability of the appearance of noise sources in the silicium substate), for larger chip surfaces, practical limits are set upon the degree of integration achievable.

A meaningful second possibility with the given technological assumptions is the multichip technique. This technique is characterized by assembling several chips on one substrate, which contains the necessary connections as vaporized or printed guide paths. In its essence it is less an element technology than more a practical connection technology of uncapped semi-conductor block switching circuits. It represents a new quality in packing technology. /210

A typical central unit of the computer generation that is currently being produced contains about 18000 integrated monolithic elements with chips of the switching circuit method. Their grating connections are led out and only connected functionally in the next higher connection plane. In addition to these integrated elements there are an additional 4200 (approximately) discrete elements, expecially sieve condensors. Thus

there are a total of about 250,000 element contacts to be connected, to be connected especially via many-layer-plates. The portion of the element contacts in the total number of necessary connecting elements, however, amounts to only about 33%. I.e., for this type of integration 2/3 of the wiring must be carried by plug connectors, back-wiring, and apparatus capping. By placing several chips and their direct function wiring in a multichip element, the number of necessary element contacts and plug connector contacts in the instrument decreases. Simultaneously a significant savings in printed circuit board surfaces becomes possible.

According to investigations of Thomas (1) on typical plug units of the central unit of the processing computor R 4000, the advantages shown in Fig. 1 arise for varying multichip element variations. The elimination of outer electric auxiliary elements such as building block contacting, circuits and plug connectors, as well as their replacement by internal building block connecting elements produced in the collective process of switching, guaranties a significant increase of the functional security of the instruments and plants. The gain in reliability in the first variation is primarily based on the reduction of the total element connection

	Multichip elements with		
	2...3 Chips	4...6 Chips	7...10 Chips
Reducing the total number of contacts of the elements by	50 ± 5 %	70 ± 5 %	76 ± 1 %
Reducing the total printed circuit board area by	40 ± 10%	50 ± 10%	60 ± 10%
Possible combining of plug units for constant printed circuit board area	2	3	4
Reducing the total number of plug connections by	15 ± 10%	25 ± 10%	35 ± 10%
Improving the failure rate by	9 %	14 %	16 %

Figure 1. Reducing the assembly expenditure when transferring from monolithic elements to multichip elements, via the example of Thomas (1) of logie plug units of the processing computer R 4000.

numbers, and for the third variant is based mainly on the decrease of the total plug connecting number. Here, however, the necessary contact number per plug unit increases, and for the first variant already makes necessary a 135 pole plug connector. For higher degrees of integration we must then have plug connectors of the conventional type of connecting numbers connected in pairs, or many at a time, to the plug unit.

In the multichip technique one may however not overlook that with increasing chip number per element, the repeatability tends to zero and is essentially restricted to the appropriate plug unit. This function-specific arrangement has significant /211
repercussions on the testing, repairing, and maintanance of replacement elements, and it needs a detailed economic discussion. The cost effectiveness of the use of multichip-elements was proved by Franck(2). From Fig. 2 we see that upon transferring to multichip elements with 8 standard chips of the switching circuit method with 3 integrated grids each, a cost reduction of about 10% in plug units and of about 20% in panels, compared with monolithic elements, is obtainable. This is in spite of an increase of the cost of the elements of about 15%. For these cost comments it was assumed that the chips are connected

via a two-plane structure with a basis of ceramic, wire-contacted to a hermitically capped element. From these calculations one may derive that an economic examination of the use of multichip elements remains incomplete if it only takes into account one element. This is because cost savings only are effective in higher connection niveaus because of a decrease of the expense for the wiring. A maximal cost reduction on panels is obtainable when the back wiring -multilayer conducting plate can be dispensed with completely due to the use of corresponding highly integrated multichip elements. For an appropriate constructive form of multichip elements, we must consider the problems of assembly of such elements on printed circuit boards, as well as their compatibility with respect to assembly technology of integrated elements that are already present. With respect to the possibility of line-up on printed circuit boards, there is an upper limit for the connection number of plug elements of 50. According to investigations by Gurth(3), in such an elements one may accomadate a maximum of 25 chips. For the construction of multichip elements in a DIP casing, a one-row chip configuration is best fitted to the geometry of the casing. For a circuit grating on the wiring carrier larger than 0.2 mm, 12 to 16 chips may be set up. The number of element contacts is then

in the range of from 40 to 50. Because of the non-optimum placing of the wires on the long side, for larger chip numbers a many-row chip configuration should be chosen. For a reliability-oriented discussion of the idea of an instrument it is however not to be recommended to work with such high degrees of integration. Investigations have shown (1) that the optimal chip number should be about 5. Then for a circuit grating larger than 0.2 mm, on the wiring carrier for these elements we would consider a DIP casing with a one-row chip configuration, with 16 to 22 connections, and with a row grating of 12.5 mm. With these values the necessary indications for technological development work are sufficiently well determined.

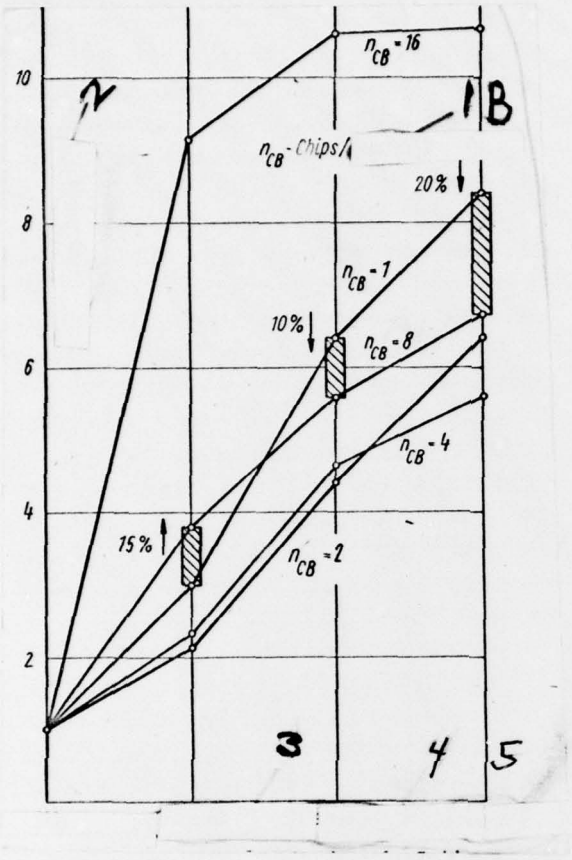

Fig. 2 Development of costs per grating, from chips up to the panel level for different multichip element variations, according to Franck (2)

1B - Element; 2- Cost units; 3- Element; 4- Plug unit; 5- Panel.

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Verfasser: Doz.Dr.-Ing.H.-J. Hanke
Technische Universität Dresden
Sektion Elektronik-Technologie
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8027 Dresden, Mommsenstr. 13

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